<center>CLAIMS</center>

What is claimed is:

1   1.   A successive approximation analog-to-digital

2 converter comprising:

3   an analog sample and hold circuit;

4   a switched capacitor DAC having an input coupled to an

5 output of the sample and hold circuit;

6   a comparator having an input coupled to an output of the

7 switched capacitor DAC;

8   a plurality of set-reset latches, each set-reset latch

9 being responsive to a combination of control signals and the

10 output of the comparator and providing non-overlapping switch

11 driver signals as set-reset latch outputs;

12   the switch driver signals being coupled to control the

13 switched capacitor DAC.

1   2.   The converter of claim 1 wherein the switched

2 capacitor DAC is a differential switched capacitor DAC.

1   3.   The converter of claim 1 further comprised of a

2 controller coupled to provide the control signals.

1   4.   The converter of claim 3 wherein the controller is

2 a state machine.

<center>16</center>

1   5.   The converter of claim 1 wherein the set-reset

2   latches have switch driver signal outputs that are level

3   shifted in comparison to the combination of control signals

4   and the output of the comparator.

1   6.   The converter of claim 1 wherein the set-reset

2   latches are NOR gate based latches.

1   7.   The converter of claim 1 wherein the set-reset

2   latches are NAND gate based latches.

1   8.   The converter of claim 1 wherein the set-reset

2   latches are hybrid logic gate based latches.

1   9.   The converter of claim 1 wherein the switched

2   capacitor DAC is a binary coded DAC.

1   10.   The converter of claim 1 wherein the switched

2   capacitor DAC is a reduced radix DAC.

1   11.   The converter of claim 1 wherein the switched

2   capacitor DAC is a mixed radix DAC.

1   12.   A successive approximation analog-to-digital

2   converter comprising:

3   an analog sample and hold circuit;

4   a differential switched capacitor DAC having an input

5 coupled to an output of the sample and hold circuit;

6   a comparator having an input coupled to an output of the

7 switched capacitor DAC;

8   a plurality of set-reset latches, each set-reset latch

9 being responsive to a combination of control signals and the

10 output of the comparator and providing non-overlapping switch

11 driver signals as set-reset latch outputs; and,

12   a controller coupled to provide the control signals;

13   the switch driver signals being coupled to control the

14 switched capacitor DAC.

1   13.   The converter of claim 12 wherein the set-reset

2 latches have latch outputs that are level shifted in

3 comparison to the combination of control signals and the

4 output of the comparator.

1   14.   The converter of claim 12 wherein the set-reset

2 latches are NOR gate based latches.

1   15.   The converter of claim 12 wherein the set-reset

2 latches are NAND gate based latches.

1   16.   The converter of claim 12 wherein the set-reset

2 latches are hybrid logic gate based latches.

1   17.   The converter of claim 12 wherein the switched

2   capacitor DAC is a binary coded DAC.

1   18.   The converter of claim 12 wherein the switched

2   capacitor DAC is a reduced radix DAC.

1   19.   The converter of claim 12 wherein the switched

2   capacitor DAC is a mixed radix DAC.

1   20.   In a successive approximation analog-to-digital

2   converter, the improvement comprising:

3   a plurality of combined set-reset latches and switch

4   drivers responsive to a combination of control signals and

5   the output of a comparator to provide successive

6   approximation switch signals to a switched capacitor DAC,

7   each combined set-reset latch and switch driver having a set-

8   reset latch having switch driver signals as latch outputs.

1   21.   The improvement of claim 20 wherein the set-reset

2   latches having switch driver signals as latch outputs have

3   latch outputs that are level shifted in comparison to the

4   inputs to the set-reset latches.

1   22.   A method of providing latched non-overlapping

2   switch driver signals comprising:

3   providing a set-reset latch responsive to latch control

4   signals referenced to a first voltage;

5   powering the latch at a second voltage different than

6   the first voltage;

7   coupling non-overlapping signals within the set-reset

8   latch as non-overlapping switch driver signal outputs.

1   23.   The method of claim 22 wherein the second voltage

2   is higher than the first voltage.

1   24.   The method of claim 22 wherein the non-overlapping

2   signals are non-overlapping in the positive logic sense.

1   25.   The method of claim 22 wherein the non-overlapping

2   signals are non-overlapping in the negative logic sense.

1   26.   The method of claim 22 wherein the non-overlapping

2   signals comprise two non-overlapping signals in the positive

3   logic sense and two non-overlapping signals in the negative

4   logic sense.